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PATTERSON & SHERIDAN, LLP
Gero McClellan / Infineon / Qimonda
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

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DOAN, DUC T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set for in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 2/8/07 has been entered.

Status of Claims

Claims 1-22 have been presented for examination in this application. In response to the last office action, the drawing(s) have been amended, claims 1,10,17,21-22 have been amended, As the result, claims 1-22 are pending in this application.

The amended drawing overcomes the drawing objection in the previous office action.

All rejections and objections not explicitly repeated below are withdrawn.

Claims 1-22 are rejected.

Applicant's arguments filed 1/9/07 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained, with changes as needed to address the amendments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,10,17,21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Bando (US 2002/0145930) and in view of Nakamura (US 6898683).

As in claim 1, Bando describes a data memory circuit, comprising: a plurality of addressable memory cells (Bando's Fig 3: memory array's cell); a command-decoding device for decoding external commands (Bando's Fig 3: #12); a control device for controlling and initiating operations on the memory cells in response to the decoded external commands (Bando's Fig 3: #26 controller receiving decoded external command RDP, WRP); and a command buffer-storing device (Bando's Fig 3: #14 buffer storing external command) for buffer-storing an external command received in a critical operating state period during which execution of the external command is impermissible and for releasing the command for execution after end of the critical operating state period (Bando's Fig 3: #23 buffering and storing external command; Bando's paragraphs 32-35 describes holding the external commands in #14 while executing the internal refresh command, and then executing the external command after the internal refreshing command is completed; see Fig 1), Bando does not expressly disclose the claim's aspect of command buffer device receives from the control device a multi-bit status signal. However, Nakamura discloses a memory control device having circuitry that indicates the critical operating state period and type of critical operating state (Nakamura's Fig 8: refresh entry mode indicates

critical period of refreshing operations of a memory refreshing type such as refresh command), Nakamura further discloses multi-bits status signal are provide to the command buffer device (Nakamura's Fig 8: #CLK1z, #CLK2z, #CLK1x, #CLK2x are provided to command buffer device comprising Fig 2: #1 command input buffers, #13, #24 command latch, #14 address buffer, #16, #22, #28). It would have been obvious to one of ordinary skill in the art at the time of invention to include critical status signal as suggested by Nakamura in Bando system that reduces power to unused circuitry depending on the critical of operations, thereby to further optimizing the power consumption of the overall system (see Nakamura's column 10 lines 5-33).

As in claim 2, Bando discloses a plurality of critical operating states are possible, and in one or more critical operating states, a set of commands is impermissible; and the command buffer device includes a buffer circuit assigned to each individual command of the set of impermissible commands (Bando's paragraph 30 describes circuit of Fig 2 buffering external commands in various critical operation states, for example when memory device executes refresh operation, read and write commands are not permitted). Bando further discloses the various critical operating states such as refresh request during standby period, and refreshing request during an operating period, see Bando's paragraph 4).

As in claim 3, Bando discloses each buffer circuit comprises: a state evaluation circuit, responsive to the multi-bit status signal, for generating a buffer standby signal during at least one operating state that is critical for the execution of respective impermissible command (Bando's paragraph 40 describes control circuit Fig 2: #20 includes logic/signal to hold the second read command during the execution of the refresh command), and a logic circuit for setting a bi-stable element into a first state when the assigned command appears while the buffer standby signal is

active and for re-generating the assigned command after the buffer standby signal has ended (Bando's paragraph 41 describes the read command is held back in the holding circuit and being re executed when the refresh operation is completed).

Claims 10,17,22 rejected based on the same rationale as of claim 1.

As in claim 21, the claim recites a method for controlling the execution of commands in a memory device comprising a plurality of addressable memory cells, the method comprising: receiving an external command while the memory device is performing a critical operation making execution of the external command impermissible; buffering the external command until the device completes the critical operation; and then executing the command. The claim rejected based on the same rationale as of claim 1. Bando's paragraphs 10,35 further describe the circuit to prevent the collision between the internal and external commands.

Claims 4-7,8-9,11-16,18-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Bando (US 2002/0145930), Nakamura (US 6898683) as applied to claims 3,1,10,17 and further in view of Kirihata (US 6404689).

As in claim 4, the claim recites wherein the command decoding device comprises: a predecoder, which, for each received command, activates a command line assigned to the received command (Bando's Fig 2: #12);

and an end decoder which excites selected enable lines of the control device depending on which of the command lines is activated. and wherein each buffer circuit is connected to a respectively assigned command line between the predecoder and the end decoder to receive the

command from respective command line and to apply a re-generated command generated to respective command line.

Bando does not explicitly shows the output driver circuit (corresponding to the claim's end decoder) at the output of the latch that stores the command (corresponding to the claim's buffering circuit). However, Kirihata describes a refresh circuit as shown in Kirihata 's Fig 6, that buffering and storing the external command until a critical operation is completed (Kirihata 's Fig 6: #624 latch transfers data to #623 latch; subsequently when xfer signal #685 is activated, data is transferred from #623 to ADDI address bus of a memory device, column 6 lines 37-66; predetermined timing period0). It would have been obvious to one of ordinary skill in the art at the time of invention to include the buffering and forwarding circuits as suggested by Kirihata in Bando's system thereby external memory commands can be held and subsequently execute in a pipeline manner (Kirihata 's column 5 lines 25-35).

As in claim 5, Bando does not expressly discloses the claim's detail of forwarding command. However, Kirihara discloses each buffer circuit includes a switch in a path of the respective command line, wherein the switch is opened precisely while a buffer standby signal is active to inhibit forwarding of an activation of the command line effected by the predecoder to the end decoder (Kirihata 's Fig 6 discloses xfer signal functions as a switch that opening or closing a path in order to transfer and to forward the information in latch #623 (corresponding to the claim's predecoder to latch #621 (corresponding to the claim's end decoder) during the execution of critical refresh command).

As in claim 6, Bando discloses a source of external commands is adapted to a specification of the data memory circuit with regard to command-issuing times (Bando's Fig 2,

Fig 3: #20a, control circuit determines when to issue the external commands based on the critical time period of the refresh operation for the specific data memory circuit/device) commands to the memory device), Bando does not expressly disclose the claim's aspect termination of internally controlled processes. However, Kirihata further discloses the command buffer device handles external commands whose execution leads to termination of internally controlled processes in the data memory circuit (Kirihata 's column 5 lines 35-50 describes a method wherein an activate command will leads to an execution and completion of an internal refresh operation in an automatic manner).

As in claim 7, the claim rejected based on the same rationale as of claim 6. Kirihara further discloses the termination refresh operation includes self refresh operation (see Kirihara's column 1lines 58-61).

As in claim 8, Bando discloses the control device includes blockage elements for blocking execution of commands during the critical operating state period (Bondo's paragraph 41, read pulse is held in th holding circuit until the refresh operation is completed), Bando and Nikamura do not expressly disclose the claim's aspect of forwarding commands. However, Kirihara further discloses the command buffer device directly forwards commands received during the critical operating state period. (Kirihata 's Fig 6 shows the xfer signal will not forward the information in latch #623 during the execution of refresh command, however the refresh command is being forwarded to the memory device).

As in claim 9, Bando and Nikamura do not expressly disclose the claim's aspect of forwarding commands. However, Kirihara further discloses wherein the command buffer device inhibits forwarding of the received command to the control device during the critical operating

state period (Kirihata 's Fig 6 shows the xfer signal will not forward the information in latch #623 during the execution of refresh command, therefore the command in latch #623 inhibits forwarding to the controller device's circuitry such as Kirihara's Fig 6: #630 latch).

Claims 11,18 rejected based on the same rationale as of claim 4.

Claims 12,19 rejected based on the same rationale as of claim 3.

Claims 13,20 rejected based on the same rationale as of claim 5.

Claim 14 rejected based on the same rationale as of claim 8.

Claim 15 rejected based on the same rationale as of claim 6.

Claim 16 rejected based on the same rationale as of claim 7.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

A) Regarding the remarks on page 9 for the objection of the drawing, and the claim objection, the amended drawing overcomes the drawing objection and the claim objection in the previous final action.

B) Regarding the remarks on pages 9-11, for the claim's amended limitation of "..from the control device, a multi-bits status signal...". the remarks are mooted in view of the new of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Regarding the Applicant's remark on page 10 third paragraph, Examiner maintains that Bando teaches the claim's 2 limitations as follows,

Bando discloses a plurality of critical operating states are possible, and in one or more critical operating states, a set of commands is impermissible; and the command buffer device includes a buffer circuit assigned to each individual command of the set of impermissible commands (Bando's paragraph 30 describes circuit of Fig 2 buffering external commands in various critical operation states, for example when memory device executes refresh operation, read and write commands are not permitted). Bando further discloses the various critical operating states such as refresh request during standby period, and refreshing request during an operating period, see Bando's paragraph 4).

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
3-19-07